AMENDMENTS TO THE DRAWINGS:

Applicants propose amending Figure 12a to clarify the invention. Applicants propose:

1) adding a signal line from the output of DCO 12, which outputs clock signal CKV, to an input of Phase Detection Circuit 60. Support for this amendment is found in paragraph [0033] and Figure 1 & 12b.

2) adding a signal line, coupled to receive a signal CTL_SRST, to an input of Phase Detection Circuit 60. Support for this amendment is found in paragraph [0056] and Figures 13 & 14 which show synchronous reset CTL_SRST.

3) adding a signal line, enabled to carry a mode switch signal OA_ZPR, from an output of control circuit 26 to an input of Phase Detection Circuit 60. Support for this amendment is found in paragraphs [0066-0067] and Figures 13 and 14.

4) adding a signal line, enabled to carry a signal OP_ZPR, from an output of control circuit 24 to an input of Phase Detection Circuit 60. Support for this amendment is found in paragraphs [0065 & 0067] and Figures 13 and 14.

5) adding a signal line, coupled to receive a signal CTL_MODE_P, to an input of control circuit 24. Support for this amendment is found in paragraphs [0064-0065] and Figure 13.

6) adding a signal line, coupled to receive a signal CTL_MODE_A, to an input of control circuit 26. Support for this amendment is derived from Figure 13 which shows CTL_MODE_P for the PVT oscillator controller or interface 24. This equivalency is established in [0066]. The acquisition controller 26, as described in [0068], is significantly identical to the controller 24, and has an equivalent mode switch signal. Accordingly, Figure 12a has been amended to show the CTL_MODE_P and CTL_MODE_A signals entering OP 24 and OP 26 circuits, respectively.

All proposed amendments to Claim 12a are illustrated in red ink. No new matter has been added. Applicants respectfully request approval.

REMARKS/ARGUMENT

Applicants recently discovered three typographical errors and have amended the specification at paragraphs [0036], [0040], and [0056], as set forth above.

As noted by the Examiner, Figure 1 does not disclose a mode switch as noted by the Examiner. Accordingly, this feature has been canceled from Claims 1 and 9.

The Examiner requires that "the phase detection circuit responsive **to a startup control signal**, as recited in claims 2 and 10, be shown or the features canceled from the claims. Applicants respectfully respond that the "startup control signal" is the synchronous reset CTL_SRST in Figure 14 (and Figure 13) – equivalency described in [0066]. As such, it is already shown in the drawing figures.

The Examiner also requires that "the plurality of phase calculators generating phase output, circuitry for combining said phase outputs", recited in claims 3-4 and 11-12, be shown or the features canceled from the claims. Applicants respectfully respond that these limitations are shown in Figure 14. The circuit in Figure 14 is part of the reference accumulator 62, which is part of the phase detection circuit 60. The first part is established in [0059]: "includes a reference phase accumulator 62" and the second part is established in [0069]: "which can be part of the reference accumulator 62". It is important to note that the phase detection circuit 60 includes the phase detector 68. The plurality of phase calculators in Figure 14 consist of adder 86 with register 90 and adder 92. The phase calculator outputs are generated at outputs of adders 86 and 92 and appear at input to multiplexer 88. This is described in [0069]. Since the "multiple phase calculators" are described in the specification to be part of the phase detection circuit 60, Applicants believe that there is no benefit of showing it graphically in Figure 12a. Nevertheless,

Figure 12a has been amended to add mode switch signals OP_ZPR and OA_ZPR which enter the phase detection circuit 60 from the OP 24 and OA 26 circuits, respectively, to better illustrate the invention.

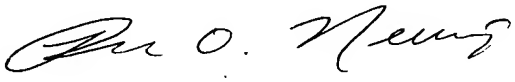
The Examiner yet further requires that "one of said phase calculator responsive a mode switch, generating its outputs from the other phase calculators," as recited in claims 5 and 13, be shown or the features canceled from the claims. The recitation "mode switch" in Claims 5 and 13 has been amended to instead be "mode switch signal". With this amendment, Claims 5 and 13 are illustrated in the embodiment of Figure 14. The mode switch signals are signals OP_ZPR or OA_ZPR. "One of said phase calculators ... generates its phase output" (output of adder 86) "from the phase outputs of the other phase calculators" (output of adder 92). This happens when the selection of multiplexer 88 transitions from 1 to 0, so that output of the second phase calculator appears at the adder 86 thus affecting the first phase calculator.

Applicants further propose amending Figure 12a to clarify the invention. Figure 12a shows more details and more actual interconnects between the digitally-controlled oscillator 12, plurality of control circuits 24-30, and the phase detection circuit 60 than does Figure 1. While a "mode switch signal" is not shown in Figures 1 or 12a, it is shown in Figure 13 as CTL_MODE_P for the PVT oscillator controller or interface 24. This equivalency is established in [0066]. The acquisition controller 26, as described in [0068], is significantly identical to the controller 24, and has an equivalent mode switch signal. Figure 12a has been amended to show the CTL_MODE_P and CTL_MODE_A signals entering OP 24 and OP 26 circuits, respectively. No new matter has been added. Applicants respectfully request approval.

Applicants propose adding new dependent claims 17 and 18. Claim 17 further defines Claim 1 and is supported by Figure 12a, as amended. Claim 18 further defines Claim 9 and is also supported by Figure 12a, as amended. No new matter has been added.

Applicants appreciate the Examiner's determination that the application is in condition for allowance except for the formal matters noted above. Claims 1-18 stand allowable over the references of record. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



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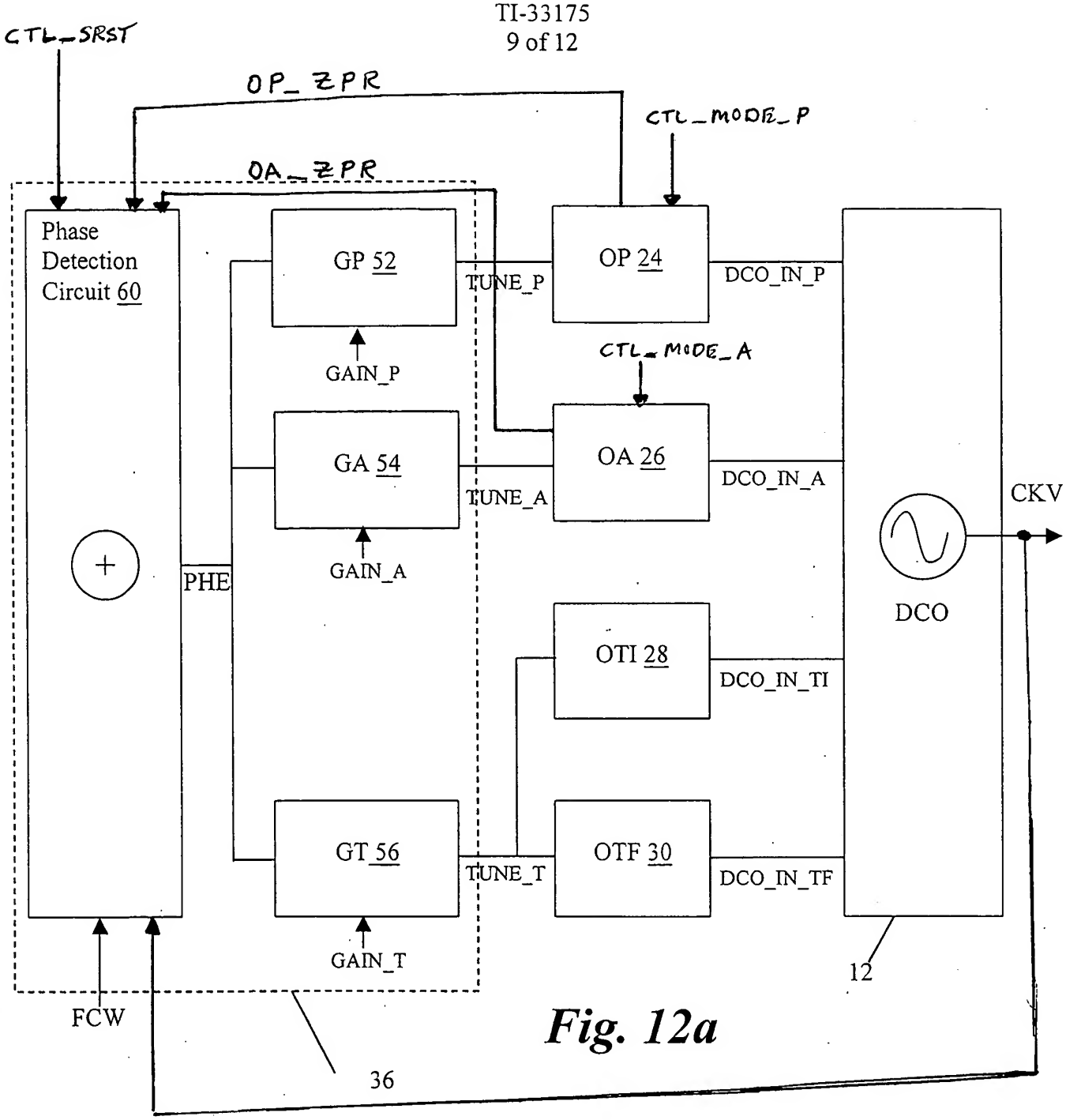

Fig. 12a